A Novel Compressive Sensing Architecture for High-Density Biological Signal Recording

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***Abstract*—The massive amount of data recorded by dense electrode arrays which are routinely connected to Nyquist-sampling signal conditioning blocks introduces new design challenges for implantable and wireless biological signal acquisition. Five different architectures of implantable multichannel neural recording systems are compared in terms of power and area constraints. Silicon results of a 16-channel spatial-domain compressive recording system implemented in a UMC 0.18 μm CMOS technology are presented. Applying intracranially recorded EEG signals, the proposed system achieves up to 16-times compression rate, consuming an extra compression power of 0.95 μW within a die area of 0.008 mm^2 per channel.**

I. Introduction

Wireless multichannel implantable interfaces for biological signal acquisition (e.g. EEG, ECG or EMG) face technological limits due to the high overall data rate which results in increased transmission power. It is crucial to implement appropriate data reduction methods within the sensors, in order to satisfy the power and area constraints of the implanted device. Compressive sensing (CS) [1] is an emerging compression method which enables the low-complexity universal encoding of sparse biological signals into a low-dimensional measurement space. Applying a random projection on-chip is significantly less costly than conventional data reduction methods such as principal component analysis, discrete wavelet transform and Huffman coding.

The previously explored single-channel approach to CS consists of on-the-fly compression of consecutive samples of each recording channel over time, either prior to [Fig. 1(a)] [2] or following [Fig. 1(b)] [3] the digitization. The amplified and filtered signal of each channel passes through m multiplication and integration paths, performing the matrix multiplication $y = \Phi x$ by which the d-dimensional signal x is mapped into an m-dimensional measurement vector y with a compression ratio of d/m, i.e., $m \ll d$. Employing CS leads to a significant data reduction of the system. However, a microelectronic architecture based on single-channel CS occupies a considerable die area when compared to the Nyquist-sampling alternatives.

To overcome the issue of area overhead inherent to the previous CS topologies, a new multichannel measurement scheme [Fig. 1(c)] is proposed which encodes data originating from every 16 channel of the array into a single compressed data stream. In the proposed approach, the compression is carried out in the discrete-time domain, and involves an spatial-domain integration of the randomly modulated samples from several channels. This technique circumvents the need to place the entire compression block within each channel and results in a compact die area in addition to significant power saving. A system-level comparison of performance in terms of power consumption and area usage is presented followed by circuit implementation and experimental results of the proposed architecture.

II. Power and Area Considerations

The associated power and area cost to different neural recording schemes are compared in this Section. The Analog single-channel CS (ACS) [Fig. 1(a)], the Digital single-channel CS (DCS) [Fig. 1(b)] and proposed Multichannel CS (MCS) [Fig. 1(c)] topologies, as well as the Conventional non-compressed array (Conv.) and the commonly used Time-Division Multiplexing-based array (TDM) are studied. In a conventional topology, each recording channel consists of an analog front-end and an individual Nyquist sampling ADC. In a TDM architecture, one single ADC with a high sampling rate converts the data originating from several channels in a multiplexed way. The following equations represent the dominant terms contributing to the power consumption of the studied topologies:

$$P_{Conv.} \approx P_{TDM} = N(P_{AFE} + P_{ADC} + P_{TX}) \quad (1)$$

$$P_{ACS} = N(P_{AFE} + \frac{P_{ADC} + P_{TX}}{CR} + m \cdot P_{INT}) \quad (2)$$

$$P_{DCS} = N(P_{AFE} + P_{ADC} + \frac{P_{TX}}{CR}) \quad (3)$$

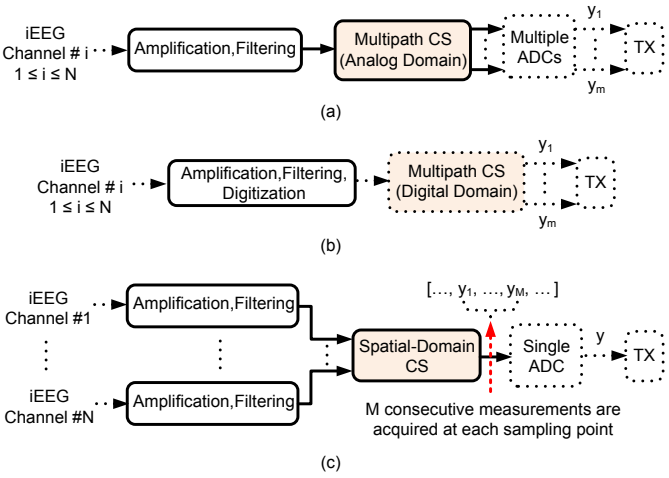

Fig. 1. Block diagram of (a) the analog single-channel CS, (b) the digital single-channel CS and (c) the proposed multichannel CS architectures.

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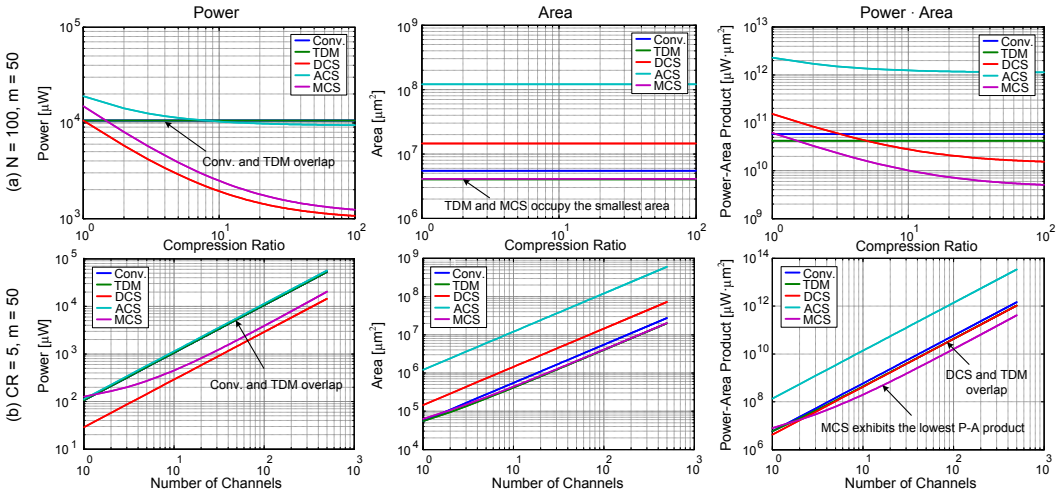

(c) Design Parameters for Power and Area Calculations

Parameter	Value
VDD	1.2 V
P_{AFE}	9.6 μW
P_{ADC}	0.1 μW
P_{TX}	96 μW
P_{INT}	1.7 μW
A_{AFE}	220 μm×180 μm
A_{ADC}	150 μm×100 μm
A_{C0}	14.2 μm×14.2 μm
A_{OTA}	150 μm×50 μm
C_0	200 fF

Fig. 2. Power, area and power-area product of several recording methods for (a) $N = 100$ and $m = 50$ and (b) $CR = 5$ and $m = 50$. (c) A set of design parameters for power and area calculations in 0.18 μm CMOS technology, according to an optimized design presented in Section III. A typical mid-band gain of 40 dB for the LNA is assumed. The compression ratio of ACS and DCS is varied by sweeping the dimension (d) of the signal per compression block.

$$P_{MCS} = N\left(P_{AFE} + \sqrt{N}(\frac{1}{CR} + \frac{1}{N})P_{ADC}\right) + \left(\frac{8 + \log_2(\sqrt{N})}{8}\right)(1 + \frac{N}{CR})P_{TX} + (1 + \frac{N}{CR})P_{INT} \quad (4)$$

where N is the number of channels and P_{AFE} is the power consumed by the analog front-end, mainly the low-noise amplifier, which is assumed identical in all topologies[1].

The compression ratio (CR) is defined as the ratio between the dimension (d) of the signal and the number of measurements (m) in the ACS and DCS topologies, and the ratio between the number of channels (N) and the number of measurements (M) in the MCS method. P_{ADC} is the power consumption of a single ADC with a sampling rate of 4 kS/s and an ENOB of 8, assuming a common figure-of-merit (FOM) of 100 fJ/conversion-step for state-of-the-art ADCs used in low-to-moderate resolution and sampling rate applications. P_{TX} is the power consumption of the transmitter that exhibits an energy-efficiency of 3 nJ/bit (assumed similar to [3] for the sake of comparison) and a sampling rate of 4 kS/s, considering an 8-bit per sample data stream. P_{INT} is the power consumption of the integrator in the ACS topology, whereas it represents the power consumption of the summing stage in the MCS. P_{INT} is mainly proportional to the bandwidth of the OTA used for integration and therefore to the frequency of random sequences applied for random sampling.

The following equations approximate the area resource demanded by the presented methods:

$$A_{Conv.} = N(A_{AFE} + A_{ADC}) \quad (5)$$

$$A_{TDM} = N \cdot A_{AFE} + A_{ADC} \quad (6)$$

$$A_{ACS} = N(A_{AFE} + m \cdot A_{ADC}) + N \cdot m \cdot A_{ENC,A} \quad (7)$$

$$A_{DCS} = N(A_{AFE} + A_{ADC}) + N \cdot m \cdot A_{ENC,D} \quad (8)$$

$$A_{MCS} = N \cdot A_{AFE} + N^{1/4} \cdot A_{ADC} + A_{ENC,M} \quad (9)$$

where A_{AFE} and A_{ADC} are the area of the analog front-end and ADC. The area of a compact SAR ADC with attenuated capacitive DACs and differential inputs is approximated by $A_{ADC} \approx 4 \cdot A_{C_0} \cdot 2^{B/2}$, with B being the number of bits [5]. The required resolution of the single ADC in the MCS topology is equal to $8 + \log_2(\sqrt{N})$ [4]. Thus, the area of the ADC is scaled by a factor of $N^{1/4}$. In each case, A_{ENC} is the total area corresponding to the integrators, digital accumulators or summing stage (depending on the compression method) and the random sequence generators. For DCS, we have used the die area information presented in [3]. The analog integrator for ACS and the summing stage for MCS are assumed to include the OTA and the sampling/integrating capacitors, based on the architecture presented in Fig. 3. Thus, the area is proportional to $2 \times 2A_{C_0} + A_{OTA}$ for ACS and $2 \times (N+1)A_{C_0} + A_{OTA}$ for MCS, where the doubling factors result from the differential implementation. The area of the transmitter is not included in the calculations since the data acquisition and transmission modules are routinely implemented into separate integrated circuits. The parameter values are shown in Fig. 2(c).

Power consumption and area usage metrics of a multichannel recording array with respect to the compression ratio (CR) and the size of array (N) are shown in Fig. 2. Considering the power and area constraints in implantable systems, one relevant figure-of-merit is the power-area product which is plotted in the figures of the third column. These figures indicate the superior performance of CS schemes compared

[1]For simplicity, the effect of the limited headroom at the output of the integrator (see [3]) on the noise performance and power consumption of the LNA and ADC in an ACS topology has been ignored. Therefore, (2) is an underestimated representation of power for an ACS-based topology. Unlike ACS, in the MCS topology, the summation occurs over a smaller number of N channels, and not over the signal dimension of d. The imposed effect [4] is less serious and is reflected in the second term of (4).

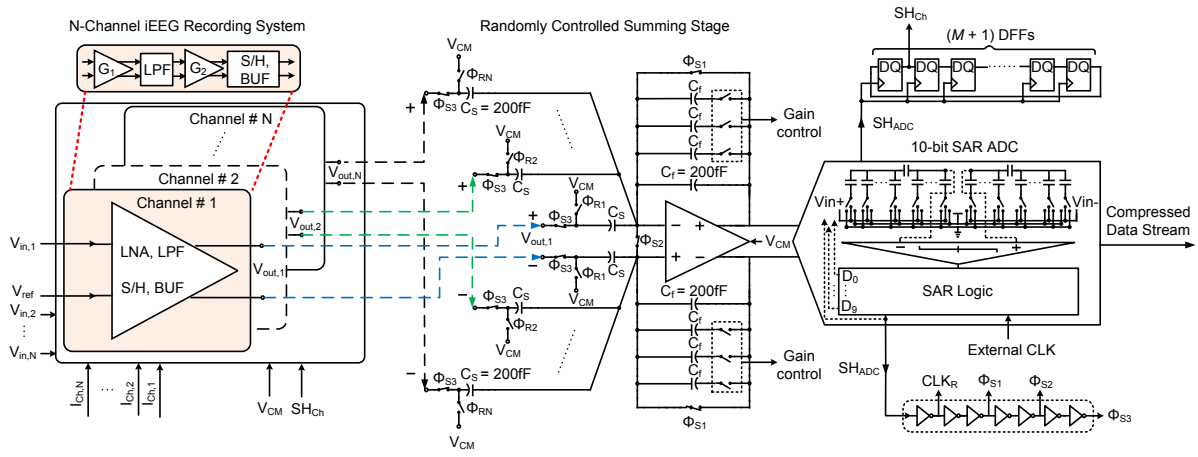

Fig. 3. Circuit implementation of the proposed multichannel CS architecture including the individual channels, the randomly controlled summing stage and a 10-bit SAR ADC.

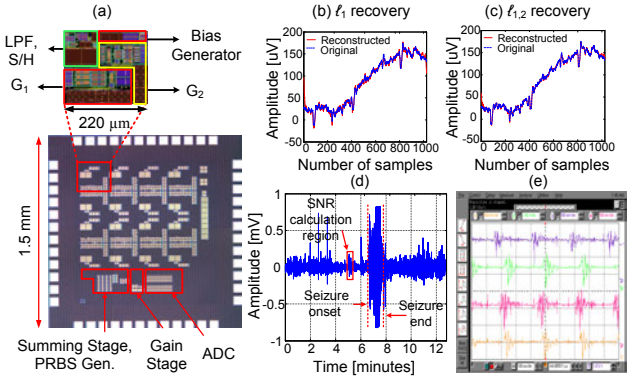

Fig. 4. (a) Microphotograph of the chip and an individual channel's layout. (b), (c) Comparison of recovery performance using different reconstruction methods for a compression ratio of 4; (b) ℓ_1 recovery, $\text{SNR}_{\text{CH1}} = 21.3$ dB; (c) $\ell_{1,2}$ recovery, $\text{SNR}_{\text{CH1}} = 28.04$ dB. (d) One channel of human intracranial EEG recording using strip and greed electrodes implanted on the left temporal lobe. (e) Sample measured four-channel iEEG signal applied from an FPGA to four channels of the chip.

to conventional and TDM topologies, in terms of power consumption. This improvement involves the penalty of additional die area. We observe that ACS and DCS require a relatively large die area. However, MCS achieves a comparable die area to TDM, in addition to its significant power efficiency. While the power saving of DCS is larger compared to MCS at small number of channels [Fig. 2(b)], this predominance diminishes for large array sizes (e.g. for $N > 20$). Still, the area efficiency of MCS justifies its superior performance over other discussed CS methods in a high-density recording system.

III. Microelectronic Architecture

The proposed MCS architecture is designed and implemented in a 1P6M 0.18 μm CMOS technology [Fig. 3]. Each of the 16 channels [Fig. 4(a)] consists of an area-efficient T-network based low-noise amplifier [6] with a band-pass transfer function, an additional low-pass filter to limit the high cut-off frequency, a second capacitively coupled gain stage, and a buffered sample-and-hold circuit. The sampled signals of N channels of the array connect to the summing stage at the sampling phase (Φ_{S3}) which follows the two in-phase events Φ_{S1} and Φ_{S2}. In sampling mode [Fig. 5(a)], Φ_{S1}, Φ_{S2} and Φ_{S3} are on, allowing the differential voltage across the two sampling capacitors (C_S) at the output of each channel to track the differential output voltage of that channel. In summation mode, the charge stored on the sampling capacitors of those channels configured with a random value equal to one are transferred to the capacitors in the feedback path (C_f). The output of the summing stage at the rising edge of the Φ_{S3} represents the randomized summation of the channels' samples which must be converted to the digital bit stream, using the ADC.

In the proposed scheme, the data sampled from a channel is kept constant during M randomized summations and consecutive digitizations by the ADC [Fig. 5(a)]. Multi-output random sequence generation (Φ_{R1},...,Φ_{RN}) is achieved by XORing the multiple outputs of maximal-length pseudo-random binary sequence (PRBS) generators [4]. All the required signals are generated using a single external clock of 400 kHz. Based on system-level requirements, an ADC with 10 bits of resolution and a sampling rate of 20 kS/s translates into a data recorded in each channel with 8 bits of resolution and a sampling rate of 4 kS/s. A binary-weighted capacitive array with attenuation capacitor is used which enables the compact implementation of the ADC.

IV. Experimental Results

The microphotograph of the fabricated chip is shown in Fig. 4(a). The total current consumption of the chip is 140 μA drawn from a 1.2 V power supply (8.75 μA per channel). The measured performance summary of the AFE and ADC is presented in Table I.

In order to measure the performance of the system in terms of reconstruction SNR, a long segment of multichannel iEEG signal recorded from subdural strip and greed electrodes implanted on the left temporal lobe of a patient with medically refractory epilepsy has been used as the input. The signals

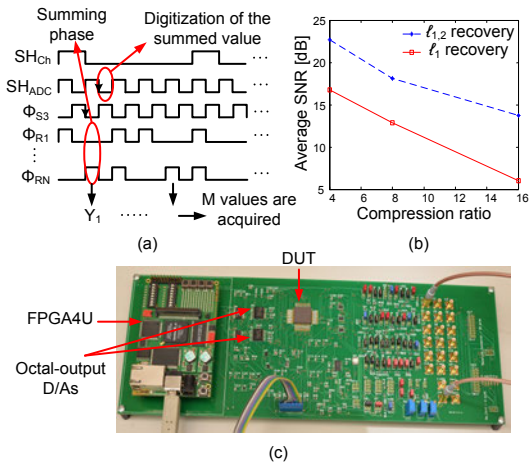

Fig. 5. (a) Timing diagram of the proposed CS system. (b) Comparison of mixed norm and sparse recovery performance for different compression ratios. (c) Measurement setup using the FPGA4U development platform for clock and pre-recorded iEEG signal generation.

TABLE I
AFE AND ADC PERFORMANCE SUMMARY.

Parameter	[8]	[9]	[6]	[10]	This Work
Technology [μm CMOS]	0.13	0.18	0.35	0.13	0.18
Bandwidth [Hz]	0.023-11.5k	10-7.2k	1-8.5k	1-5k	39-1.9k
Gain [dB]	38.3	39.4	38.1	54-60	43.8
Input-Ref. Noise [μV_{rms}]	1.95	3.5	13.3	5.1	4.2
NEF	2.48	3.35	7.87	4.4	4.12
AFE Power [μW]	12.5	7.92	6	8.5	9.4
ADC Sampling rate [kS/s]	10-100	-	-	$\leq$100	20
ENOB	6.2	-	-	7.6	9.2
ADC Power [μW]	< 1	-	-	1.5	2.6

recorded by 16 adjacent channels of electrodes (arranged in greed formation) are applied to the proposed CS system. The iEEG signal is generated using an FPGA based platform. The FPGA transfers preloaded serial iEEG digital data to two off-chip eight-channel D/A converters [Fig. 5(c)]. Gabor transform is employed as the sparsity domain of neural signals for multichannel neural recovery based on sparse and mixed norm methods [4]. The recovery SNR of the reconstructed signal ($\hat{x}$) with respect to the original signal (x) is calculated for each recording channel. The mean SNR of 16 channels are averaged over 100 blocks of the signal, as shown in Fig. 4(d). The performance of the circuit is validated for low-voltage fast activities which are shown to be associated with seizure onset. The reconstructed signals versus the original signals corresponding to one block of a single channel data using ℓ_1 and $\ell_{1,2}$ recovery are shown in Fig. 4(b) and (c). The length of each compression block (d) is equal to 1024 samples and is equivalent to 256 msec at a 4 kHz sampling frequency. The digitized data after ADC is used for recovery. As shown in these figures, applying the $\ell_{1,2}$ recovery on the compressed data produced by the adjacent channels results in an improved recovery performance, compared to the sparse recovery. The averaged SNRs using the ℓ_1 and $\ell_{1,2}$ recovery are 16.64 and 21.80 dB, respectively. Reducing the number of measurements to $M = 1$, i.e. $CR = 16$ results in average SNR of 13.72 dB, using $\ell_{1,2}$ recovery. Thus, the system is able to successfully

TABLE II
COMPARISON OF SYSTEM PERFORMANCE WITH PUBLISHED LITERATURE.

Parameter	[3]	[7]	[11]	This Work
Compression method	DCS	PWL Spike det.	DWT Spike det.	MCS
Number of channels	1	1	32	16
Comp. area/chan. [mm^2]	0.103	0.080	0.18	0.008
Comp. power/chan. [μW]	1.9	1.18	95	0.95
Sampling rate/chan. [kS/s]	$\leq$20	90	25	4
Compression ratio	$\leq$10	125	$\leq$20	$\leq$16

recover low-voltage iEEG signals compressed applying a ratio as high as 16 (i.e. one randomly accumulated sample is acquired from 16 channels). The average reconstruction SNR for sparse and joint recovery for different compression ratios is shown in Fig. 5(b). Table II summarizes the performance of the system and presents a comparison with published works.

V. CONCLUSION

The theory of compressive sensing has been used as a powerful data compression method for sparse biological signals. A new 16-channel compressive sensing architecture is implemented which enables 16-times data compression of the conventional Nyquist-rate iEEG recording system, resulting in 16-times power reduction at the transmitter. The proposed approach is a suitable choice for power- and area-constrained implantable devices.

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