Jitter Analysis and Measurement in Subthreshold Source-Coupled Differential Ring Oscillators

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***Abstract*—The jitter and the phase noise of ring oscillators utilizing subthreshold source-coupled logic (STSCL) style are analyzed in this paper. Closed-form equations are derived to predict the jitter and phase noise caused by white and flicker noise. Measurement results of a test chip fabricated in a standard CMOS 90 nm technology are presented to validate these expressions. The performed analysis shows that jitter in STSCL-based ring oscillator is independent of technology parameters, as opposed to its CMOS counterparts that depend on supply voltage and parameters of technology. Based on measured results, noise on current control line can dominate the total jitter of the oscillator. Design guidelines are proposed to limit the jitter effect of ring oscillators using STSCL logic. The proposed STSCL-based ring oscillator achieves an average RMS jitter as low as 0.24 % of the oscillation period at a 1.08 MHz/μA energy efficiency, which demonstrates its suitability for ultra-low-power applications.**

I. Introduction

Recently, the subthreshold source-coupled logic (STSCL) topology has been introduced as an alternative circuit approach for implementing ultra-low-power digital systems (see Fig. 1) [1]. In this type of logic circuits, the input differential pair is biased in subthreshold regime. Thanks to the control of the tail bias current, the power consumption of each logic gate can be reduced even below the leakage of a single transistor [1]. In CMOS logic, the gate delay, the energy consumption and the noise performance have a tight inter-dependence through circuit and process parameters, which can heavily constrain the circuit optimization [2]. On the other hand, the design of STSCL gates is more relaxed mainly thanks to the independence of delay to supply voltage, and to device parameters such as threshold voltage (V_{TH}) and gate oxide thickness (t_{ox}). Accordingly, STSCL logic circuits permit to choose the optimal device and circuit parameters targeting a minimum energy consumption level without affecting the gate delay. This improved flexibility makes system level design and power management easier to handle and more effective, when aggressive requirements on the consumption are targeted.

In this paper, the jitter and phase noise of ring oscillators based on STSCL topology are analyzed. As shown in the following, jitter has little dependence on global process parameters and supply voltage. The differential implementation guarantees the immunity of the ring oscillator to supply noise. As shown in [3], device mismatch can substantially affect the performance of STSCL circuits. Therefore, a variation-aware device sizing is required to guarantee proper circuit operation and performance in large-scale and mass produced implementations with adequate parametric yield. We finally provide some design insights for proper implementation of STSCL-based ring oscillators.

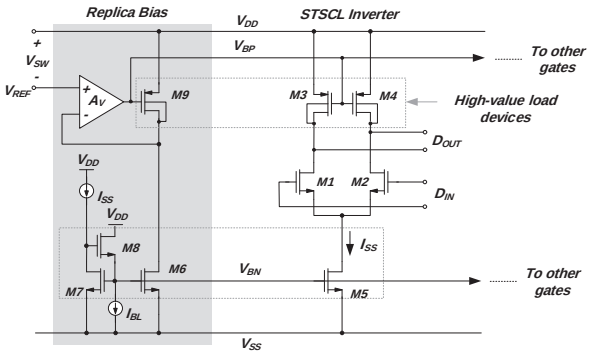

Fig. 1. A subthreshold SCL gate and its replica bias circuit used to control the output voltage swing [1].

This paper is organized as follows. Section II provides an overview on STSCL circuits. The jitter and phase noise are analyzed in Section III. The experimental results to validate the theoretical findings are presented in Section IV, and Section V concludes the paper.

II. STSCL Circuits: Fundamental Properties and Design Guidelines

The circuit schematic of an STSCL inverter is shown in Fig. 1. The operation of STSCL circuits is similar to the conventional SCL (or current-mode logic, CML) circuits [4]. In this topology, the logic operation takes place in current domain based on the polarity of the input signal, D_{IN}. Then, the output current is converted back to voltage domain (D_{OUT}) by the load resistances. Very high-value load devices are required since current levels are extremely low (as low as few pico-Amperes) in STSCL topology. As depicted in Fig. 1, these load resistors can be implemented using drain to bulk shorted PMOS devices [1]. A simplified circuit diagram of the replica bias (RB) circuit used to control the output voltage swing is also shown. The replica bias circuit generates the bias voltage for the NMOS tail transistor and the PMOS load devices.

The transconductance of a differential pair circuit operating

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in subthreshold regime can be estimated by [1], [5]:

$$G_m = \frac{\partial I_{OUT}}{\partial D_{IN}} = (\frac{I_{SS}}{2n_n U_T}) \cdot \frac{1}{\cosh^2(D_{IN}/(2n_n U_T))} \quad (1)$$

where D_{IN} indicates the input differential voltage, n_n is the subthreshold slope of the NMOS devices, and U_T stands for the thermal voltage. Based on (14), for $D_{IN} > 4n_n U_T$ the entire tail current will be switched to one of the output branches. Therefore, a voltage swing of more than $4n_n U_T$ is needed to guarantee that the gain of the STSCL circuit is sufficiently large to be used as a logic gate. The value of the load resistance can be estimated by:

$$R_{SD} = \frac{n_p U_T}{I_{SD}} \cdot \frac{e^{V_{SD}/U_T} - 1}{(n_p - 1)e^{V_{SD}/U_T} + 1} \quad (2)$$

where n_p is the subthreshold slope of PMOS devices [1]. Combining (2) with (14) results in [1]:

$$A_V = G_m \cdot R_{SD} \leq \frac{n_p}{n_n \cdot (n_p - 1)}. \quad (3)$$

A bias control circuit is necessary to keep the voltage swing at the output of STSCL gates at a desired value. Indeed, a reduction in VSW leads to a degradation in the noise margin, whereas an increase in VSW determines proportional gate delay increase. Hence, V_{SW} should be selected close to its optimum value. A replica bias circuit is employed for this purpose. The schematic of the replica bias circuit has been shown in Fig. 1. The replica bias circuit needs to be sufficiently precise. Thus, the amplifier A_V in Fig. 1 should provide enough gain with a very low offset to guarantee the desired accuracy. The STSCL gate used inside the replica bias circuit should be well matched to the STSCL gates being biased to ensure operation at the targeted operating point. In general, a high enough value for V_{SW} should be selected in order to compensate the effect of variation at the output voltage swing and keep the NM on acceptable level.

It has already been shown that one single replica bias circuit can be shared across a large number (e.g. several hundreds) of STSCL gates, so that its area and consumption can be amortized over a large number of logic gates. The level shifter implemented by M_8 and I_{BL} in Fig. 1, keeps the drain voltage of M_7 sufficiently large to operate at high enough V_{dsat} (overdrive voltage) levels and avoid entering into triode region, even at very low bias currents.

The power dissipation of an STSCL-based digital system with an average logic depth of N per pipeline stage is:

$$P_{diss,STSCL,N} \approx \ln 2 \times N^2 V_{DD} V_{SW} C_L f_{op} \quad (4)$$

where C_L stands for the average load capacitance at the output of STSCL gates and f_{op} indicates the system operation frequency [1]. The delay of each STSCL gate can be approximated by:

$$t_d = \ln 2 \times R_L \cdot C_L \approx \ln 2 \times (V_{SW}/I_{SS}) \cdot C_L \quad (5)$$

where I_{SS} is the tail bias current of each cell. Considering (4) and (5), it can be concluded that the device parameters including the threshold voltage, do not influence the speed-power consumption tradeoff in SCL topology. The replica bias circuit will compensate for the effect of temperature and process variations [1]. Therefore, this topology exhibits a very low sensitivity to PVT or global variations [3].

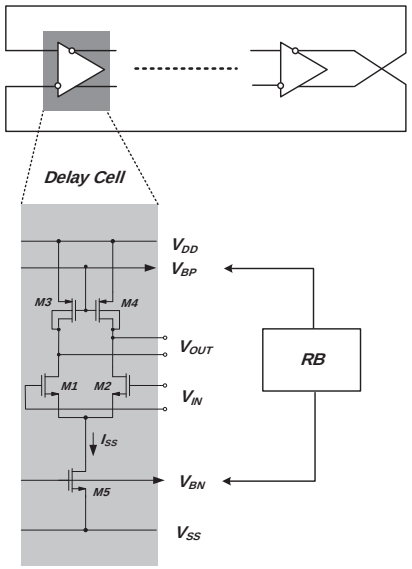

Fig. 2. Differential STSCL-based ring oscillator.

III. Jitter Analysis

Jitter is an undesired effect which changes the instantaneous oscillation frequency of an oscillator. The oscillation frequency of the STSCL-based ring oscillator shown in Fig. 2 is controlled by the bias current I_{SS} according to the following linear relationship:

$$f_0 \simeq \frac{I_{SS}}{2 \ln 2 N_d V_{SW} C_L} \quad (6)$$

where N_d is the number of delay elements in an oscillator ring and C_L is the load capacitance at the output nodes of each delay element.

A. White Noise-Induced Jitter

Assuming period jitter as the standard deviation σ_τ of the oscillation period around its mean value and using an analysis similar to [6], the jitter of an STSCL-based ring oscillator is represented as:

$$\sigma^2_{\tau,STSCL} = 2N_d \frac{\langle v_n^2 \rangle}{(I_{SS}/C_L)^2} \quad (7)$$

where $\langle v_n^2 \rangle$ is composed of:

$$\langle v_n^2 \rangle = \langle v_{n,load}^2 \rangle + \langle v_{n,tail}^2 \rangle + \langle v_{n,diff}^2 \rangle. \quad (8)$$

As usual, jitter can be calculated by dividing the total noise voltage by the slope of the differential switching voltage at zero crossing (I_{SS}/C_L) [3]. The white noise contributions of load resistors (M_3, M_4), tail transistor (M_5) and differential pair (M_1, M_2) are immediately found to be [6]:

$$\langle v_{n,load}^2 \rangle = \frac{2KT}{C_L} \quad (9)$$

$$\langle v_{n,tail}^2 \rangle = S_{i_{n,tail}} \frac{R}{4C_L} \tag{10}$$

$$\langle v_{n,diff}^2 \rangle = S_{i_{n,diff}} \frac{3R}{8C_L} \tag{11}$$

As opposed to the differential ring oscillator in [6], in the STSCL-based ring oscillator, the differential and tail transistors are biased in subthreshold regime. Therefore, the PSD of the thermal noise at the drain of the transistors is described by [7]:

$$S_{i_n} = 4kTG_{nD} \tag{12}$$

where G_{nD} is defined as:

$$G_{nD} = \frac{n_n}{2} G_m \tag{13}$$

n_n is the subthreshold slope factor of NMOS devices and transconductance in weak inversion is:

$$G_m = \frac{I_D}{n_n U_T} \tag{14}$$

This results in:

$$\sigma_{\tau,STSCL,wn}^2 = \frac{2kT}{I_{SS} f_0 \ln 2} \left(\frac{7}{16U_T} + \frac{1}{V_{SW}} \right). \tag{15}$$

Applying the relationship derived in [6] for phase noise versus jitter induced by white noise yields:

$$L_{STSCL,wn}(f) = \frac{2kT}{I_{SS} \ln 2} \left(\frac{7}{16U_T} + \frac{1}{V_{SW}} \right) (\frac{f_0}{f})^2 \tag{16}$$

in which V_{SW} is the differential voltage swing at the output of each delay cell and U_T is the thermal voltage.

On the other hand, for a CMOS inverter-based and a CMOS differential ring oscillator with differential pair operating in strong inversion, the predicted jitter due to white noise are [6]:

$$\sigma_{\tau,inv,CMOS}^2 = \frac{2kT}{I_{SS} f_0} \left(\frac{1}{V_{DD} - V_{TH}} (\gamma_N + \gamma_P) + \frac{1}{V_{DD}} \right) \tag{17}$$

and

$$\sigma_{\tau,diff,CMOS}^2 = \frac{2kT}{I_{SS} f_0 \ln 2} \left(\gamma_N (\frac{3}{4V_{effd}} + \frac{1}{V_{efft}}) + \frac{1}{V_{SW}} \right) \tag{18}$$

respectively. V_{effd} and V_{efft} stand for the effective gate voltage on the differential pair and tail transistor, and γ_N, γ_P are the thermal noise coefficient of NMOS and PMOS transistors, respectively.

Considering the above equations, while both (17) and (18) strongly depend on technology parameters (V_{TH} and γ), (15) is fully independent. It is also expected that the variability of the measured jitter in STSCL-based ring oscillators will be less than similar inverter-based and CMOS differential ring oscillators, due to the insensitivity of jitter to the threshold voltage. Improving the matching of the load transistors reduces the variations of V_{SW} and improve the jitter variability. In addition, in the STSCL topology, the replica bias circuit compensates the effect of temperature and process variations. By comparing the derived equations of jitter, the sensitivity of maximum jitter (i.e., the jitter at minimum V_{SW} based on (15)) to temperature is substantially smaller compared to the jitter calculated from (17) and (18), by replacing $V_{SW,min} = 4n_n U_T$ and $U_T = kT/q$ in (15).

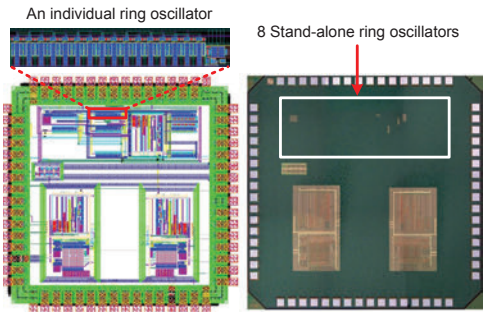

Fig. 3. Mask layout (left) and chip microphotograph (right) of the test chip in a CMOS 90 nm technology.

B. Flicker Noise-Induced Jitter

From (6), the sensitivity of oscillation frequency to tail current is $\kappa_I = f_0/I_{SS}$. The induced phase noise hence results to [6]:

$$L_{fn}(f) = \frac{\kappa_I^2}{4f^2} S_I(f) \tag{19}$$

where $S_I(f)$ is the flicker noise spectral density arising from the bias transistor (M_7) and observed in the drain current of M_5:

$$S_I(f) = A \cdot g_{m,tail}^2 \cdot \frac{K_f}{WLC_{ox}f}. \tag{20}$$

The last term in above equation stands for the flicker noise PSD referred to the gate of M_7 and K_f is an empirical coefficient [6] independent of bias and technology parameters. It is assumed that the width of the diode-connected NMOS transistor (M_7) is $1/A$ of the width of the tail NMOS transistors in the delay stages (A $\geq$ 1). Replacing (14) as $g_{m,tail}$ in (20) yields the following equation for the flicker noise induced phase noise due to the diode-connected bias transistor:

$$L_{STSCL,fn}(f) = \frac{AK_f}{WLC_{ox}} \left(\frac{1}{4n_n^2 U_T^2} \right) \frac{f_0^2}{f^3}. \tag{21}$$

It is useful to observe that (21) represents the dominant source of flicker noise in a differential ring oscillator, which is also validated in our measurements presented in the following Section.

IV. Experimental Characterization of Jitter

A test chip was fabricated in a standard CMOS 90 nm technology, to verify the above models on silicon. Several ring oscillators were implemented and placed at different distances to a common replica bias circuit. Different distances are adopted to explore the impact of mismatch, which tends to be larger at larger distances, thus determining larger jitter. To achieve the desired dynamic range, the delay mismatch among delay stages in a ring oscillator needs to be sufficiently low. Careful sizing of the load and bias tail devices were carried out to achieve the desired precision in the oscillation frequency under variations. The implemented test chip illustrated in Fig. 3 includes eight stand-alone STSCL-based ring oscillators.

In this design, the tail bias current of each delay element can be tuned from 10 pA up to 10 nA using internal programmable current mirrors. The oscillation frequency increases almost linearly with the controlling current. The voltage swing has

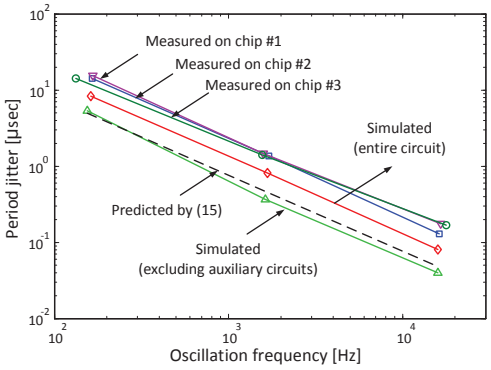

Fig. 4. Measured period jitter versus oscillation frequency for three sample chips. This is compared with prediction based on (15) and simulated jitter, with and without considering auxiliary circuits. The average measured RMS jitter is equal to 0.24 % of the oscillation period. The bias current ranges from 10 pA to 1 nA in logarithmic steps.

been set to 200 mV, which ensures adequate noise margin since it it larger than the theoretical lower bound ($4nU_T$). Each ring oscillator approximately consumes 15 times the tail bias current, since the number of delay cells is $N_d = 15$.

The measured RMS jitter versus oscillation frequency for three sample chips is shown in Fig. 4. The jitter is also simulated in two different conditions, i.e., including and excluding the noise from replica bias, current mirror and current scalers (the tail transistor is included in both cases). The predicted value based on (15) is also plotted against measurement and simulation results. Comparing the two simulation plots, one observation is that flicker noise significantly affects the jitter of the ring oscillator, as expected. This noise mainly originates from the tail and the diode-connected current mirror transistors (derived in (21)) as well as the input-referred flicker noise of the amplifier in the replica bias circuit. It is worthwhile mentioning that, as shown in [6], the white noise in auxiliary circuits and flicker noise in the differential pair do not contribute to the overall jitter and phase noise. Another reason for the difference between measured and simulated/predicted results is the effect of external noise sources such as substrate and supply noise and the noise on the frequency control current which are not taken into account in simulations and analysis. While at low frequencies, the flicker noise of the tail transistor can cause the simulated jitter to slightly exceed the predicted value only based on white noise, the opposite deviation at higher frequencies is observed. This can be explained by the fact that the above analysis is based on the assumption of complete steering of current between the two sides of the differential pair, while in subthreshold region, it is not possible to completely steer the tail bias current to either branch, which can reduce the actual noise compared to the value predicted by (15).

Replacing I_{SS} from (6) in (15) results in:

$$\sigma^2_{\tau,STSCL} \simeq \frac{2kT}{N_d V_{SW} C_L f_0^2} \left(\frac{7}{16U_T} + \frac{1}{V_{SW}} \right) \qquad (22)$$

The linear dependency of the period jitter to the oscillation period derived from the above equation is consistent with the measured and simulated results in Fig. 4. Higher frequency (and power consumption) results in smaller value of jitter. For a fixed oscillation frequency, larger values of N_d result in smaller period jitter, which at the same time requires a larger bias current and power consumption.

Interestingly, as opposed to static CMOS inverter-based ring oscillator, the oscillation frequency and jitter of STSCL oscillators are not directly dependent on the supply voltage, which guarantees a higher immunity of STSCL-based circuit to supply noise.

In addition to the speed of operation in the STSCL topology which has low dependency on process variations and can be precisely controlled through bias current, the timing jitter is also independent of the technology-based parameters. Hence, the jitter is more accurately controlled through design parameters such as I_{SS} and V_{SW}, regardless of possible variations in device parameters. Moreover, as long as the tail bias current (I_{SS}) is much higher than the junction leakage currents and V_{SW} satisfies the necessary condition for the inverter to perform as a logic gate, the oscillator can properly operate even in aggressively scaled deep sub-micron technologies. The proper matching of the load devices and sufficient bandwidth of the amplifier in the replica bias circuit are crucial aspects to minimize the variations of V_{SW} and provide stable operation of the STSCL-based ring oscillator over a wide range of operation frequencies. This improvement in performance and lower power consumption is achieved at the cost of relatively larger area usage of STSCL-based circuits compared to their CMOS alternatives.

V. Conclusions

The jitter and phase noise arising from white and flicker noise in an STSCL ring oscillator have been derived in this paper. The white noise-induced timing jitter has been shown to be independent of any device parameter, as a unique feature of STSCL ring oscillators. In practical implementations, the oscillator is inserted inside a PLL that suppresses the flicker noise, accentuating the impact of white noise. The jitter measurements of the stand-alone ring oscillators have also been presented. The predicted jitter caused by white noise agrees well with the simulation results, while measured jitter is higher due to the current control and flicker noise of the bias circuitry. The average RMS jitter is as low as 0.24 % of the oscillation period, which demonstrates the utility of STSCL based ring oscillator for ultra-low-power applications.

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