In-Vivo Validation of a Compact Inductively-Powered Neural Recording Interface

Mahsa Shoaran*, Gürkan Yilmaz†, Ramesh Periasamy‡, Stefanie Seiler‡, Stefano Di Santo‡,
Claudio Pollo‡, Kaspar Schindler§, Hans-Rudolf Widmer‡, Catherine Dehollain†, and Alexandre Schmid*
EPFL, *LSM, †RFIC, Lausanne, Switzerland
‡Department of Neurosurgery, University of Bern, Switzerland
§Department of Neurology, University of Bern, Switzerland

***Abstract*—This paper presents the electrical and in-vivo validation of a compact, low-noise and low-power integrated circuit for the acquisition of cortical signals in a high-density implantable system. Using a three-stage topology, the proposed architecture enables a compact implementation of the analog front-end, while preserving a low-noise and lower-power performance. A wireless energy transfer module is also implemented which consists of a four-coil resonant inductive link. The proposed circuit architecture is implemented in a UMC 0.18 μm CMOS technology. The analog front-end achieves a noise efficiency factor of 4.2, consuming 9.4 μW of power within an effective area of 200 μm $\times$ 200 μm per channel. The wireless power transmission link achieves an efficiency of 36% at a separation distance of 10 mm, while providing 10 mW of DC power.**

***Index Terms*—Compact, in-vivo, implantable, low-noise, high-density, wireless power transmission.**

I. Introduction

IN-VIVO monitoring of neural activity using implantable interfaces provides an efficient solution to the diagnosis and treatment of neurological disorders. Future implantable systems will include hundreds of electrodes integrated with signal acquisition circuits into flexible and biocompatible substrates [1]-[3]. Along with significant improvements in the signal processing methods and electrode fabrication technology, the power minimization of the implantable system has been widely addressed [4] to satisfy the heat generation limits of the implantable device. To realize a high-density recording system, minimizing the circuit area is also crucial which enables including a high number of recording units into the available die area.

In addition, on-site neural signal acquisition and digitization necessitates a power supply in the implant. Among various methods such as using an implantable battery, ambient energy harvesting, and wireless power transmission, the latter one is employed. Ambient energy harvesters cannot provide sufficient power and miniaturized implantable batteries need to be recharged which limits their practical implementation. Wireless power transmission can be performed using waves at different frequencies ranging from ultrasound to infrared depending on the constraints and specification of the target application. In cortical implants, the major constraints relate to the size, power transfer efficiency (PTE) and tissue absorption. Consequently, wireless power transfer has been realized by using magnetic coupling, which enables a high PTE at low MHz-range frequencies, where tissue absorption is minimal. At the sensing side, an area-efficient and low-noise signal conditioning architecture is implemented and powered in-vivo, using the proposed wireless power transmission circuit.

This paper is organized as follows. Section II presents the circuit-level implementation of the analog front-end and wireless power transmission modules. Electrical and in-vivo experimental results of the proposed architecture are presented in Section III and Section IV concludes the paper.

II. Circuit Implementation

The block diagram of the proposed system is shown in Fig. 1. The design of the analog front-end is based on minimization of the die area at a low power consumption and acceptable noise performance. In the wireless power transmission link, the power transfer efficiency and delivered output power are considered as the main design parameters.

A. Three-Stage Neural Recording Topology

The neural acquisition block amplifies and filters the weak neural signals sensed by the implanted electrodes. The proposed architecture consists of a low-noise amplifier with a band-pass transfer function, a low-pass filter stage to limit the high cut-off frequency and a second gain stage to provide additional amplification of input neural signal.

In this design, a three-stage configuration is used [5] in order to minimize the total die area of a channel and provide the desired amplification and filtering of the input signal.

1) Low-Noise Front-End Gain Stage G_1: An area-efficient T-capacitor network-based amplifier [6] is used as the front-end gain stage G_1, which provides a mid-band gain of 29.8 dB (Fig. 1). The gain of this stage is realized by multiplying two capacitive ratios. This technique provides a high closed-loop gain in a single stage. The total size of the capacitors employed in this topology is smaller than the size of capacitors in a conventional capacitive feedback topology [7].

The differential mid-band gain of this stage is calculated as

$$A_M = -(\frac{C_1}{C_2})(\frac{2C_4 + C_2 + C_3}{C_3}) \quad (1)$$

The second capacitive ratio in (1) is selected small compared to the first term, to satisfy the low-noise operation of G_1 [3]. In this design, $C_2 = C_3 = 200$ fF, $C_1 = 1.4$ pF and

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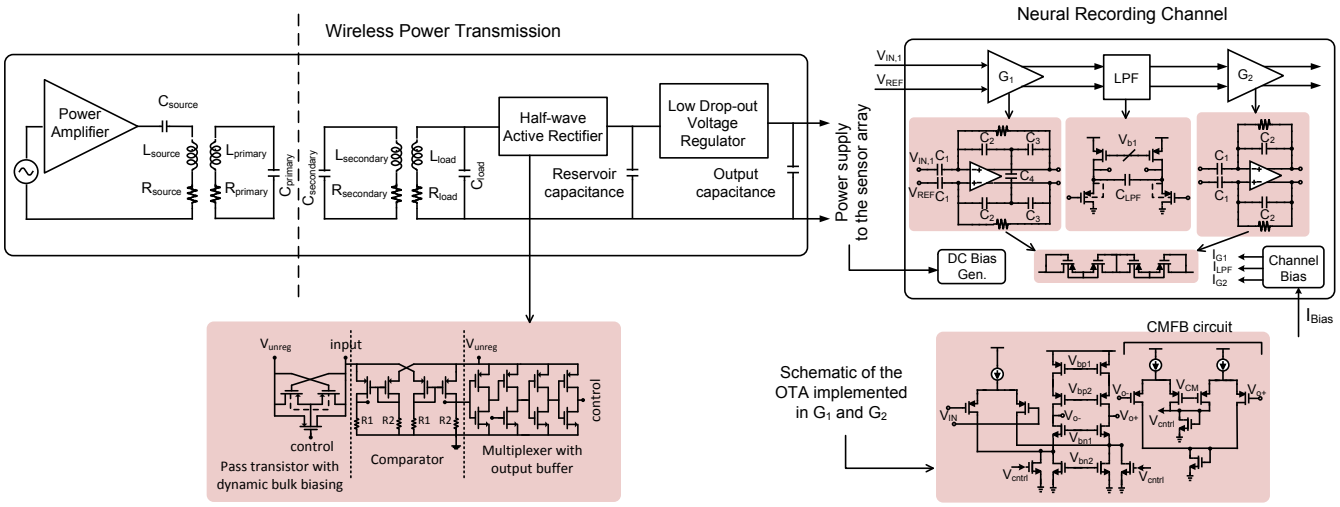

Fig. 1. Block diagram of the proposed neural acquisition system including the wireless power transmission block and a low-noise signal conditioning module.

$C_4 = 400$ fF, resulting in $C_{tot} = 4$ pF. The conventional capacitive feedback topology [7] requires a total capacitance of 64 $\times$ 200 fF $\approx$ 12.8 pF to achieve a similar mid-band gain. Thanks to the small input capacitance of the selected topology, the attenuation effect of cortical signals at the interface of the electrode and acquisition channel is alleviated.

A folded-cascode OTA with a continuous-time common-mode feedback (CMFB) circuit is implemented in the LNA (Fig. 1). The total bias current of the OTA is 7 μA. The simulated passband of the LNA ranges from 28 Hz to 144 kHz. The linearity performance of the LNA is described by the THD metrics which is 0.24% for a 2 mV_{p-p} input signal. The LNA consumes 8.4 μW of power (VDD = 1.2 V), corresponding to 89% of the total power consumed by the channel.

Four back-to-back MOS devices biased in subthreshold region are used to implement the high-value feedback resistors with sufficient linearity for creating a low-frequency high-pass pole (Fig. 1). Owing to the series connection of the high-value resistors in a symmetric combination, the equivalent resistance exhibits symmetric variations around the quiescent point in all process corners.

The ac-coupled architecture provided by the capacitive feedback topology enables the amplifier to reject the large dc offsets (as large as 1-2 V [7]) which are commonly generated in an electrode-tissue interface. The common centroid layout of the input differential pair in the LNA and the passive components such as input and feedback capacitors results in improved matching and offset performances, which are mainly limited by the front-end LNA. The measured input-referred offset of the stand-alone channel is 0.85 μV.

2) Low-Pass Filter Stage: In order to limit the amplification bandwidth of the channel at a minimal power and area overhead, a first-order source-follower based low-pass filter (adapted from [8]) is used which achieves sufficient linearity at a small bias current (Fig. 1). The DC-gain loss due to the bulk transconductance which is inherent to the source-follower architecture is reduced by a source-to-bulk connection. The internal feedback of the source-follower circuit and processing the signal in voltage domain increases the linearity range of the filter. The presented filter exhibits a THD of 0.08 % (equal to 10-11 bits of linearity) for a filter input signal of 60 mV_{p-p} (or 2 mV_{p-p} at the input of a channel) consuming a bias current of 5.4 nA. The cut-off frequency is 1.9 kHz and is tunable by the current.

3) Second Gain Stage G_2: A second gain stage (G_2 in Fig. 1) provides an additional gain of $A_{M2} = 13.64$ dB using a conventional capacitive feedback architecture. The power consumption of the second gain stage is negligible (0.72 μW) compared to the front-end LNA, thanks to the relaxed noise requirements. Using a folded-cascode OTA architecture, an output voltage swing as large as 200 mV_{p-p} is achieved in the second gain stage. The size of the transistors in this OTA are selected smaller compared to the OTA used in the front-end LNA, thanks to the relaxed noise and matching requirements.

B. Wireless Power Transmission

The wireless power transfer chain has been established from a 4-coil resonant inductive link which is terminated with a rectifier and a voltage regulator at the implant side (Fig. 1). Since the power transfer efficiency and the power dissipation at the implant side are the major concerns in neural recording applications, the design of each block has been optimized to obtain maximum power transfer efficiency. It is worth to note that the overall efficiency of the system can be accurately approximated as the multiplication of the efficiency of each block.

Recent studies have shown that using 4-coil instead of 2-coil resonant inductive link in biomedical remote powering yields a significant increase in the power transfer efficiency. The inductive link driven by an AC source creates an AC voltage at the output terminals of the load coil at the implant side. However, a reliable DC supply is required to supply the

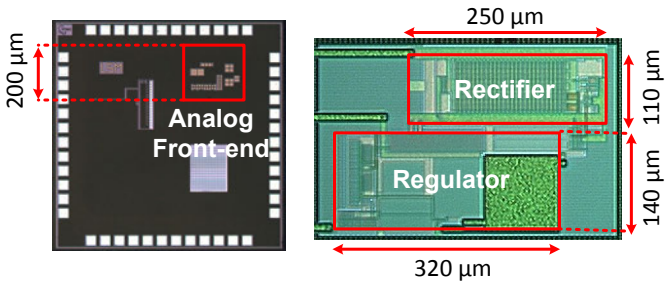

Fig. 2. Microphotographs of the neural recording channel and wireless powering chips.

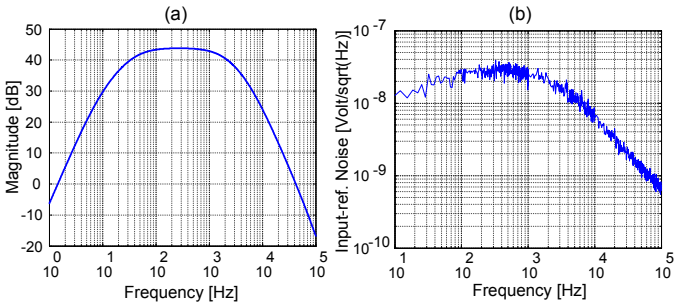

Fig. 3. (a) Measured frequency response at the output of G_2 and (b) measured input-referred noise of the neural recording channel.

electronic circuits in the implant. Therefore, a half-wave active rectifier has been employed to convert AC to DC since it enables a lower voltage drop compared to full-wave versions and its active comparison mechanism outperforms passive rectifiers, particularly as the output power increases. Since the output of the rectifier still contains ripples, a low-drop-out voltage regulator has been designed and implemented in order to provide a reliable DC supply for the electronics of the neural recording system. The voltage reference of the regulator is integrated on chip by modifying a cascoded bootstrapped current source. The error amplifier is implemented using a single-stage operational transconductance amplifier topology.

A performance characterization of the powering system alone is carried out with a separation distance of 10 mm and an operation frequency of 8.5 MHz. The rectifier is connected to the inductive link and the combined efficiency is measured at 46% while the rectifier output power is approximately 13 mW. The measurement is repeated with connected regulator, and the overall power efficiency from the input of the inductive link to the regulator output has been measured as 36% for a 10 mW output power and a 1.8 V DC output voltage. The overall power transfer efficiency can be approximated by multiplying the individual efficiencies of the inductive link, the rectifier, and the regulator (55%, 82%, and 78%).

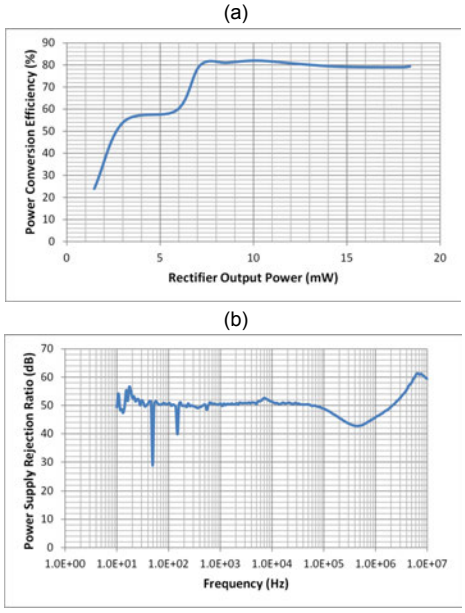

Fig. 4. (a) Measured power conversion efficiency of the rectifier with respect to the output power and (b) power supply rejection ratio of the low drop-out voltage regulator.

III. Experimental Results

The proposed system is designed and implemented in a 1P6M 0.18 μm CMOS technology. The microphotographs of the implemented neural recording channel and power transmission modules are shown in Fig. 2. The designed rectifier and regulator occupy a silicon area of 300 μm $\times$ 250 μm. The recording channel is implemented within an effective area of 200 μm $\times$ 200 μm.

A. Floating Microelectrode Array (FMA)

The implanted 16-channel electrode array (Alpha Omega GmbH, custom made) consists of sixteen recording and two additional reference and ground electrodes tethered to a connector by a thin, flexible and light-weight cable (Fig. 5(a)). The array is floating and is not anchored to the skull. The cable includes Parylene-C insulated gold wires. The platform housing the individual microelectrodes is fabricated from alumina ceramic which has been laser-machined to pattern 18 holes distributed with 400 μm separation. The electrodes are platinum/iridium. The electrode shank diameter is 75 μm and the recording electrode impedance is larger than 100 kΩ. The length of the electrodes is 2 mm. The length of the cable is 15 cm to preserve sufficient distance between the animal and the recording board which is connected through the appropriate Omnetics connector to the matching connector at the extremity of the array. The total size of the substrate including the electrodes is 2.5 mm $\times$ 1.95 mm.

B. Surgical Procedure for Implantation of the Electrode Array Into a Rat Brain

Two adult male Wistar rats weighing 300-400g (Janvier, France) were deeply anaesthetized by isoflurane inhalation (75% N_2, 20% O_2, 5% isoflurane) followed by intraperitoneal injection of narketane (ketaminum; 75 mg/kg body weight) and xylapane (xylazinum; 5 mg/kg body weight) and analgized by subcutaneous injection of buprenorphine (0.5 mg/kg).

Subsequently the rat was mounted on a stereotaxic frame (Stoelting) and subcutaneously injected with a local pain killer (Lidocain HCL 1%, 0.2 ml). The head was shaved and disinfected before the midline incision was made. The scalp was opened and held with micro-clamps. Two burr holes were drilled at the following coordinates (in relation to the bregma): A/P = +1 mm and -0.4 mm respectively, M/L = -2 mm, and the dura was carefully removed. The electrode reaching 2 mm into the cortex was positioned at the following coordinates (in relation to the bregma): A/P = +0.5 mm, M/L = -2.5 mm (Fig. 5(b) and (c)). Animal experiments were approved by the Animal Research Ethics Committee of the Canton Bern, Switzerland.

C. Electrical and In-Vivo Validation

The measured frequency response at the output of G_2 and the input-referred noise of the recording channel are shown in Fig. 3(a) and (b). The high-pass pole is measured at 39 Hz. The input-referred noise density at the channel input is 25 $nV/\sqrt{Hz}$ at 1 kHz. The input-referred noise integrated over the signal bandwidth is 3.2 μV_{rms}, while it increases to 4.2 μV_{rms} when integrated from 1 Hz to 100 kHz. The Noise Efficiency Factor (NEF) of the analog front-end (including G_1, LPF and G_2) is defined as [9]:

$$\text{NEF} = V_{n,rms} \cdot \sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \qquad (2)$$

The measured NEF is equal to 4.12 and 3.23 for the noise integration bandwidths of 1 Hz-100 kHz and passband of the signal, respectively.

The power conversion efficiency of the rectifier is measured with respect to the output power while maintaining the DC level of the output voltage at 2.2 V, as depicted in Fig. 4(a). The graph in Fig. 4(b) shows the power supply rejection ratio of the regulator. The regulator provides a suppression of 50 dB around DC and 60 dB around the operation frequency of 8.5 MHz. The load regulation is calculated at 0.15 % for an output power range from 1 mW to 10 mW.

Intracranial EEG signals were successfully recorded from the setup presented in Fig. 5(a)-(d), using the wireless-powered low-noise front-end. The extracellularly recorded action potentials are shown in Fig. 5(d) and (e).

IV. Conclusion

The experimental and in-vivo validation of a compact low-noise neural recording system are presented. The implemented recording channel is supplied by a wireless power transmission circuit. The wireless energy transfer is realized using magnetic coupling and the corresponding power generation circuits are implemented on-chip. The area efficiency realized by a three-stage topology and low noise operation confirm the relevance of the proposed approach for high-density recording applications, at a pitch as small as 200 μm.

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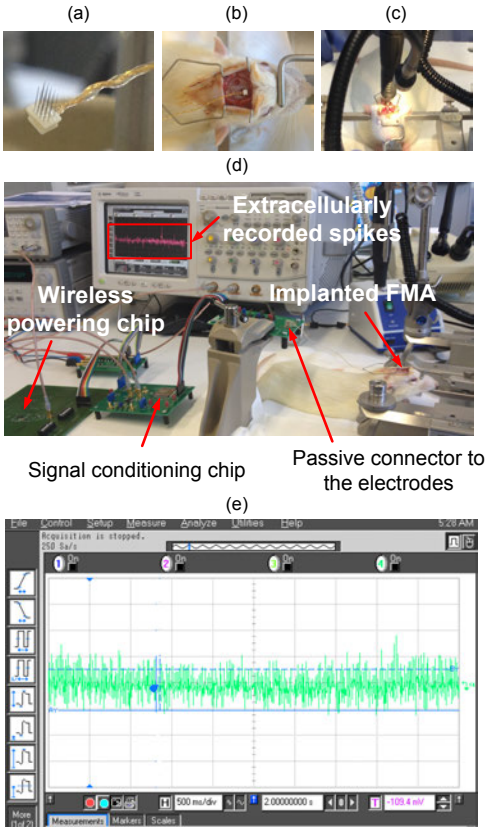

Fig. 5. Experimental validation of the proposed system; (a) floating microelectrode array; (b), (c) implanted electrodes in a Wistar rat brain; (d) measurement setup for in-vivo experiments, and (e) extracellularly recorded neural signal.

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