A Fully Integrated IC With 0.85-μW/Channel Consumption for Epileptic iEEG Detection

Mahsa Shoaran, *Student Member, IEEE*, Claudio Pollo, Kaspar Schindler, and Alexandre Schmid, *Member, IEEE*

***Abstract*—Feature extraction from a multichannel compressed neural signal is introduced in this brief. Compressive sensing (CS) is an efficient method for reducing the transmission data rate of sparse biological signals and lowering the power consumption of resource-constrained sensor nodes. However, recovering the original signal from compressed measurements is typically achieved by relatively complex and optimization-based algorithms, which is hardly suitable for real-time applications. The previously proposed multichannel CS scheme enables the area-efficient implementation of CS. In this brief, a low-power feature extraction method based on line length is directly applied in the compressed domain. This approach exploits the spatial sparsity of the signals recorded by adjacent electrodes of a sensor array and detects the seizure onset for every sixteen channels of the array. The proposed circuit architecture is implemented in a UMC 0.18-μm CMOS technology. Extensive performance analysis and design optimization enable a low-power and compact implementation. The proposed feature extractor reaches a perfect sensitivity of 100% for 420 h of clinical data containing 23 seizures from four patients, with an average false alarm rate of 0.34 h^{-1} for artifact-free channels, consuming 0.85 μW of power/channel at a compression rate of 16.**

***Index Terms*—Compressive sensing (CS), feature extraction, intracranial electroencephalography (iEEG), seizure onset detection.**

I. Introduction

RECORDING with high spatiotemporal resolution enables neuroscientists to investigate the fine-scale electrophysiological activities within the brain and provides them with a previously unexplored insight into the mechanisms underlying neurological disorders. In epileptic patients, the submillimeter scale of high-frequency oscillations involved in seizure generation [1] motivates the wide-bandwidth recording of intracranial electroencephalography (iEEG) signals using high-spatial-resolution electrodes. As opposed to standard widely spaced ($\approx$ 1 cm) electrodes with large surface areas, the spacing and diameter of dense intracranial electrodes can be as small as 0.5 mm and 0.3 mm, respectively [2]. In addition, high-resolution electrophysiology is beneficial for patients with pharmacoresistant epilepsy, as 25% of epileptic patients. Developing a wireless implantable device capable of delivering electrical stimulation or delivering a drug upon detecting an imminent seizure can make a great impact on the quality of life of these patients [3]. It is expected that the inclusion of signals recorded from dense electrodes allows the system to improve the accuracy of seizure detection, as compared to traditional detection methods based on low-precision electrode arrays [4].

In order to preserve the benefits of high-resolution recording and satisfy the power requirements of the implantable device, appropriate data reduction methods are employed. Discrete wavelet transform [5], spike detection [6], and compressive sensing (CS) [7], [8] are the most popular approaches proposed in literature. Among these methods, CS is a computationally simple approach, which is successfully translated into circuit level [7], [8], with relatively low power consumption and high compression rate.

In order to alleviate the area cost of implementing CS in a dense array with stringent area constraints on each channel, a multichannel compression method has been recently proposed [8]. However, the speed and computational complexity of the recovery algorithm is a major drawback of CS-based approaches.

In this brief, spatial-domain CS in combination with feature extraction is proposed as an efficient method to limit the amount of data acquired by a seizure detector device. As opposed to the existing feature extraction methods, which are separately applied to each channel, the proposed method (see Figs. 1(a) and (b)) is applied to the compressed signal of a group of channels. The proposed method is compared to the raw data-domain feature extraction, particularly focusing on the seizure detection performance.

II. Current Schemes and Proposed Architecture

The previously explored on-chip solution to seizure detection consists of extracting the spectral energy of each electroencephalography (EEG) recording channel within several frequency bins [9]. The most challenging part in integrating a feature extraction block on-chip relates to minimizing the large required area and power consumption of the filter banks. Although useful techniques are introduced [10] in order to limit the area of the filter banks, the area limitation becomes extremely stringent in a high-density system recording from several channels and particularly at a high sample rate, which necessitates a higher number of filters. In this work, we propose

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M. Shoaran and A. Schmid are with the Microelectronic Systems Laboratory, Swiss Federal Institute of Technology (EPFL), 1015 Lausanne, Switzerland (e-mail: mahsa.shoaran@epfl.ch).

C. Pollo is with the Department of Neurosurgery, Bern University Hospital, 3010 Bern, Switzerland.

K. Schindler is with the Department of Neurology, Inselspital, Bern University Hospital and University of Bern, 3010 Bern, Switzerland.

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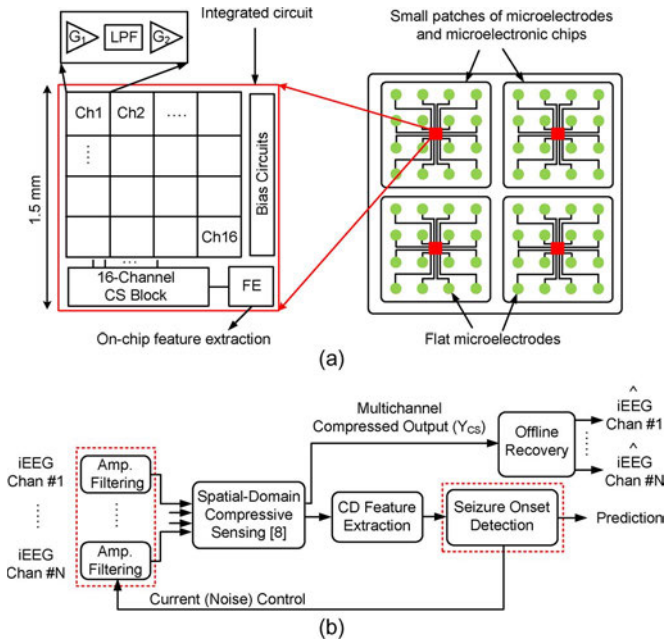

Fig. 1. (a) System-level view of the proposed method; signals recorded by every 16 electrodes are processed by a microelectronic chip. (b) Block diagram of the system; offline recovery of the compressed data provides full access to the original signals.

a method that includes the information from all channels of an electrode array and simultaneously improves the area and power efficiency by applying a low-complexity feature extraction method to a group of channels (see Fig. 1) in the compressed domain (CD).

A. MCS Technique

The proposed feature extraction method builds upon the multichannel CS (MCS) system initially presented in [8]. The CS transform is generally expressed by $y = \mathbf{\Phi}x$, where the d-dimensional signal x (e.g., EEG signal, which is shown sparse in the Gabor basis [8]) is sampled as an m-dimensional measurement vector y with a compression ratio (CR) of d/m, i.e., $m \ll d$. In the MCS model [8], the random projection $y = \mathbf{\Phi}x$ is applied to the spatially sampled values from N channels of the array. Assuming a CR of N, the individual samples of N channels are multiplied by a random value of 0 or 1 and summed together as a single measurement.

Employing MCS in hardware leads to a significant data reduction of the system and an area-efficient implementation. This approach circumvents the need to load each channel with multiple random sequences and avoids placing additional memory on the chip.

B. Signal Recovery Cost

As opposed to the simple compression model applied in CS, the signal recovery is usually achieved by nonlinear and relatively expensive optimization-based or iterative algorithms [11], generally transferring the following signal analysis (e.g., seizure onset detection) into a base station. In spite of many efforts aiming at improving the speed and accuracy of the recovery algorithms, the state of the art still lacks the capacity of real-time operation for many applications. However, in many signal processing problems, only the specific features of the signal are of interest, and the exact recovery is not necessary [11]. In order to leverage the benefits of data compression, developing algorithms that do not require the full data recovery and directly perform feature extraction and processing in the CD is potentially interesting.

C. Proposed CD Feature Extraction

The complexity of making a reasonable decision based on the single-channel detections in a dense recording array as well as the area and power overhead of implementing the in-channel feature extraction circuits necessitate an improved seizure detection strategy.

In general, many software-based seizure detection approaches employ sophisticated algorithms to increase the detection accuracy. However, the limited power and area budget of an implantable device impose strict constraints on the choice of appropriate seizure detection features. Extracting frequency-based features involves computationally intensive algorithms such as filtering and fast Fourier transform evaluation, which is hardly suitable for an on-chip implementation. Considering the hardware cost and detection accuracy, the coastline feature has been selected and extracted from the multichannel iEEG signal prior to, and following, the compression. Coastline achieves the best seizure detection performance among more than 65 different time- and frequency-domain features [12]. This feature is a measure of the line length between successive samples and provides an appropriate characteristic of epileptiform iEEG since it increases at low-amplitude fast activities as well as high-amplitude slow activities [13]. The coastline feature of block i is computed as

$$C_i = \left(\frac{1}{256}\right) \sum_{256} |x[n] - x[n-1]| \tag{1}$$

where $x[n]$ is the value of signal x at time $t_n = n \times T_{\mathrm{S/H}}$, with $T_{\mathrm{S/H}}$ being the sample-and-hold (S/H) time of the analog-to-digital converter (ADC). Normalization is done by shifting the digital feature output by 8 bits toward the LSB. The choice of the division factor (i.e., the summation window length) depends on the signal amplitude, the detection accuracy, and the required latency of detection.

III. Microelectronic Architecture

The circuit-level implementation of the proposed architecture is shown in Fig. 2. The neural signals recorded by every N electrodes of the array (N is equal to 16 in this design) are processed through amplification and filtering stages located inside the channels. The differential outputs of the channels connect to the MCS block and randomly accumulate at the single-ended output of this stage. As shown in [8], the compressed sensing system is very robust against circuit nonidealities such as noise. Thus, the compressed data stream is digitized using a

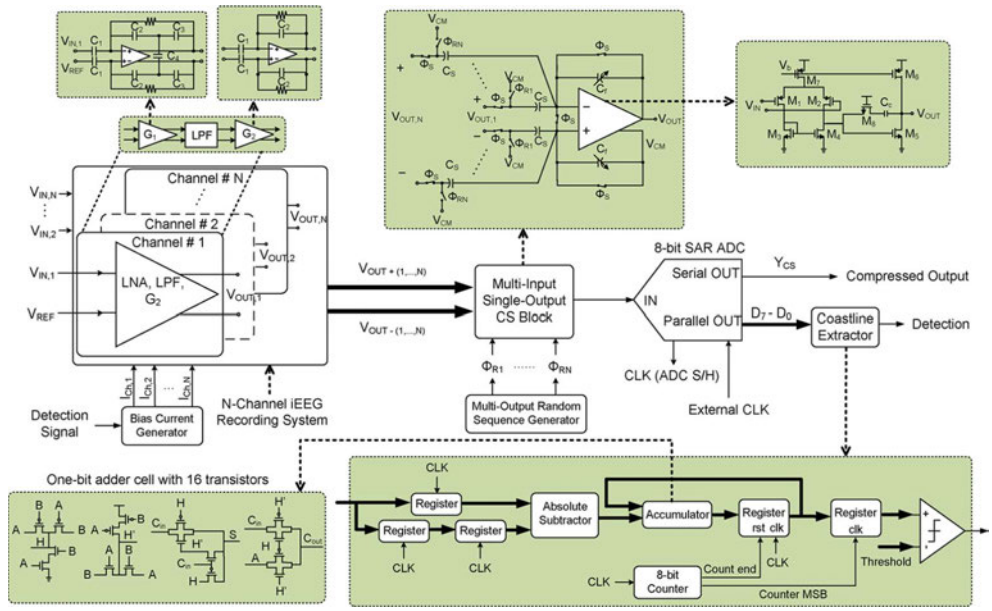

Fig. 2. Schematic of the proposed multichannel feature extractor system, including the individual channels, an MCS block with 16 differential inputs and a single output, an 8-bit successive approximation ADC, and a digital coastline extractor block.

moderate-resolution successive approximation ADC. The serial output of the ADC can be used for a full recovery of the original iEEG signal at the receiver side.

The employed CS technique enables 16 times data reduction and power saving of the transmitter, as compared to the conventional noncompressed design. The digital output is delivered to the 8-bit feature extractor block in parallel form. To improve the power efficiency of the system, the bias current of the front-end amplifiers (G_1 in Fig. 2) is doubled upon seizure detection at the output comparator of the feature extraction block. This technique avoids unnecessary power dissipation while normal (i.e., seizure-free) iEEG is being recorded. Upon seizure detection, the current of the low-noise amplifier (LNA) increases, which simultaneously reduces the input-referred noise of the channel and enhances the achievable SNR at the output.

A. Signal Conditioning Blocks

The in-channel signal conditioning circuit performs the signal amplification and filtering in a three-stage topology. This architecture efficiently optimizes the die area usage of a channel at the given gain and bandwidth requirements. Compared to [8], stringent power requirements are considered in this design, and the power supply is reduced by 33%. In addition, the S/H stage is embedded within the MCS block, alleviating the need to place a separate S/H and buffer circuit in each channel. To avoid aggressive increase of the input capacitors of the LNA, a topology similar to [14] is adapted in a differential implementation. The high-value feedback resistors are implemented by back-to-back MOS devices, which operate in the subthreshold region. The total bias current of the operational transconductance amplifier (OTA) implemented in G_1 is 0.7 μA and 1.4 μA, in the two modes of operation (normal and seizure recording). The current consumption of the OTA used in G_2 is 0.3 μA, due to the relaxed noise requirements at this stage. A folded-cascode OTA is implemented in both G_1 and G_2. Large PMOS input pair limits the flicker noise at G_1, while smaller transistors are employed at the input pair of G_2,

A source-follower-based low-pass filter consuming a total bias current of 13.8 nA is used to limit the high cutoff frequency. The total midband gain of the channel is 45.3 dB. The input signal is amplified in the frequency range of 30 Hz–1.7 kHz. This frequency range covers both ripples and fast ripples, as two types of signals that are indicators of epilepsy. These signals are discernible using high-spatial-resolution electrodes. The total input-referred noise of the channel integrated from 1 Hz to 100 kHz is 5.74 $\mu V_{\rm rms}$ and 7.07 $\mu V_{\rm rms}$, at the high- and low-biasing conditions, respectively.

B. MCS Block

The differential outputs of the channels connect to the multiple-input single-ended summing stage (see Fig. 2), as the core of the MCS block. This stage is controlled by a sampling signal (Φ_S) and N random sampling signals $(\Phi_{R1}, \ldots, \Phi_{RN})$. The random sampling signals are generated using an on-chip multiple-output pseudorandom binary sequence generator with minimal power and area overhead [8]. During sampling, the differential voltages at the outputs of the channels are sampled across the two sampling capacitors (C_S). During summation (Φ_S is off), the charge stored on the sampling capacitors of the channels with a random value equal to one are transferred to the capacitor in the feedback path (C_f). Thus, the outputs of the channels are randomly accumulated at the output of the MCS block. A two-stage OTA, which provides a rail-to-rail output swing (see Fig. 2), is used within the summing stage of the MCS block. A variable voltage gain is achieved through the 2-bit controlling switches in series with the feedback capacitors (shown as a variable feedback capacitor in Fig. 2). In order to set the appropriate value of the gain in a real *in vivo* experiment, a patient-specific training phase is required.

C. ADC and Feature Extractor

An 8-bit binary-weighted capacitive array with attenuation capacitor is employed, which enables a compact implementation of the successive approximation ADC. All the required signals are generated using a single external clock of 64 kHz. The S/H signal of the ADC is generated at a rate equal to 1/16 of the external clock, which enables 8-bit conversion of the summed value.

An 8-bit feature extractor circuit computes the coastline parameter at the output of the ADC. The block diagram of the coastline extractor is shown in Fig. 2. The multibit output of the ADC is passed through register stages, which capture two successive compressed values. The absolute difference of the two inputs is generated at the output of the subtractor and accumulated over a window length of 256. Extra bits are employed in the arithmetic hardware to prevent overflow during the accumulation. An 8-bit synchronous binary counter controls the accumulation window and resets the register after 256 consecutive additions. Within the coastline generation chain, the absolute differential value of the successive samples is shifted toward the least significant bit by 8 bits, enabling the division operation in (1). At the rising edge of the counter MSB output (with a period equal to $256/f_{\mathrm{CLK}}$), the accumulated value is compared with a trained threshold input using a digital comparator stage. The detection signal associated with the coastline parameter is raised upon exceeding the threshold value in a window length of 64 ms (see Fig. 4), at an ADC sampling rate of 4 kS/s. A low-power and low-power-delay-product 16-transistor adder cell (see Fig. 2) is employed as the main building block of the subtractor, accumulator, and comparator stages. The S-generation branch is excluded for implementing the multibit comparison. Considering the relaxed speed requirements inherent to the application, a ripple-carry adder is implemented to enable the multibit operation. The total power consumption of the ADC and feature extractor is 0.54 μW. The feature extractor occupies an area of 300 μm $\times$ 85 μm on the chip.

IV. System and Circuit-Level Validation

The proposed seizure detection method was evaluated using iEEG data from four patients with medically refractory epilepsy. The patients underwent presurgical evaluation at the Inselspital in Bern, Switzerland (see Table I). The iEEG signals were acquired using a 128-channel system and sampled at 32 kHz (Neuralynx, Inc.).

The proposed MCS method is applied to the subblocks of neighboring 16-channel iEEG signals. The coastline feature is extracted from 16 channels in each subblock and also in the CD. A moving average is applied to the extracted features. In total, 103 subblocks containing 23 seizures from four patients have been processed. The total length of the analyzed iEEG data is 420 h and includes preictal, ictal, and postictal activities.

The average sensitivity and false alarm rate (FAR) versus CR are shown in Fig. 3. Sensitivity is computed as the ratio of correct seizure predictions to the total number of registered seizures. FAR is measured by the number of false positive

TABLE I
Patient Information and Characteristics of Epilepsy

ID	Sex	Age	Seizure type	Seizure onset	Type of electrodes	No. of contacts
1	F	24	LTLE[a]	Medial Temporal Gyrus Left	Strips, Grid, Depth	54
2	M	36	MTLE[b]	Hippocampus Left	Strips, Depth	56
3	F	46	LTLE	Superior Temporal Gyrus Left	Strips, Grid	56
4	M	26	PLE[c]	Inferior Parietal Lobule Left	Strips, Grid	60

[a]Lateral temporal lobe epilepsy.
[b]Mesial temporal lobe epilepsy.
[c]Parietal lobe epilepsy.

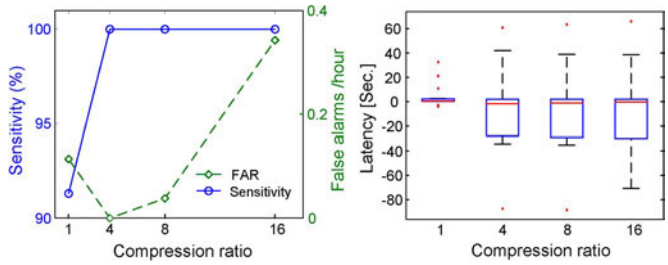

Fig. 3. (Left) Average sensitivity and FAR and (right) latency of the coastline feature versus CR.

detections in 1 h of recording. The whisker plot presented in Fig. 3 shows the latency to the seizure onset versus CR. Latency is defined as the amount of time after (or before if negative) electrographic seizure onset taken by the selected feature to cross the threshold and trigger a detection. The point CR $= 1$ corresponds to the channel-based detection. For this purpose, the median of the sorted vector formed by the 16 detection times associated with the channels of each subblock is selected. The calculated sensitivity and FAR are averaged over subblocks and patients.

As shown in Fig. 3, the sensitivity of the traditional approach based on multiple channels' detections is worse than a CD detector, which exclusively handles a single compressed data stream. The features extracted in the CD represent the grouped activity of several channels. The compressed output is a linear combination of samples recorded from adjacent channels and is a reasonable *intermediate* representative of the subblock's total activity. Using a higher number of measurements (e.g., CR $= 8$), the system is able to achieve a more accurate representation of the signal, which results in a lower false detection rate. The proposed system is easily adaptable to operate at CR $= 8$, by doubling the sampling frequency at the random summation stage and ADC. Considering the latency graph, the channel-based coastline feature is mostly concentrated around the median (zero), since its calculation method is similar to the electrographic onset definition [13] used in our analysis.

In order to assess the performance of the proposed design, multichannel recorded signals of the slices of a rat somatosensory cortex are applied to the implemented circuit. This signal includes epileptiform burst activity and extracellularly detected spikes (see Fig. 4). The seizure detection performance of the

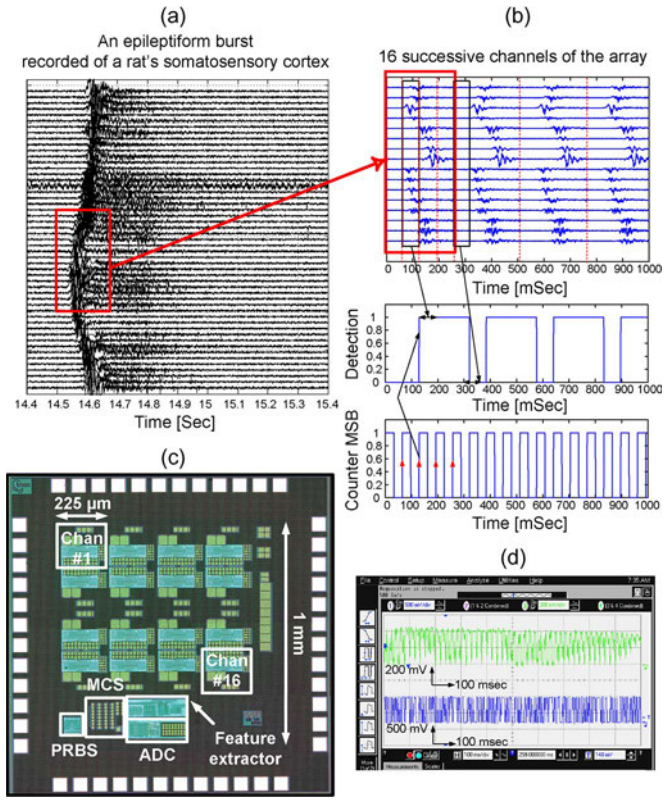

Fig. 4. (a) and (b) Measured seizure detection performance of the proposed circuit; a window of length 256 ms at the beginning of the epileptic burst is periodically applied into the circuit. Using an FPGA platform, the preloaded serial iEEG data are transferred into two off-chip eight-channel D/A converters, and the analog outputs are applied to the recording channels. (c) Die micrograph of the fabricated chip and (d) the measured compressed output and an on-chip generated random sequence.

TABLE II
PERFORMANCE COMPARISON WITH PUBLISHED WORK

	Technology [μm CMOS]	Area /channel [mm^2]	Power /channel [μW]	Sens. [%]	FAR [#/hour]	Latency [Sec.]
This work	0.18	0.0625	0.85	100	0.34	- 0.27
[3]	0.18	1.68[a]	162[b]	> 92	-	0.8
[10]	0.18	3.125[c]	> 66[d]	84.4	> 0.04	< 2
[9]	0.18	6.25	6.7	-	-	-

[a]Including telemetry, classification and stimulation / channel count.
[b]Feature extraction and classification power / channel count.
[c]Including classification engine and divided by channel count.
[d]Analog front-end power.

fabricated chip is shown in Fig. 4. A window length of 256 ms at the beginning of the epileptic burst is periodically applied to the circuit. Every 64 ms of the iEEG signal is mapped into a seizure or nonseizure event, at the rising edge of the counter MSB signal. A seizure is detected after 128 ms, which correctly represents the seizure onset time falling within the second subwindow of the signal.

The performance summary and a comparison with existing works are shown in Table II. The total current consumption of the proposed system is 17 μA, which is drawn from a 0.8-V power supply. The proposed solution incurs lower computational complexity in the feature extraction stage, due to the reduction in the number of samples processed in the CD. This computational advantage could be further enhanced by the fact that even fewer samples are required for detection purposes in the CD, than for signal reconstruction [11]. In addition, the spatial CS enables proper offline data recovery of the original physiological signal at the receiver. This feature is highly desired by physicians who prefer to have access to the entire iEEG data for a thorough clinical evaluation.

V. CONCLUSION

In the future, dense neural recording interfaces will integrate a high number of acquisition channels at high sampling rates, exacerbating the need to perform some type of data reduction at the sensors. This work represents the first fully integrated circuit that addresses the multichannel CD feature extraction. A performance comparable to the raw data-domain detector is retained up to CRs as high as 16, consuming 0.85 μW of power within a small die area. The proposed system enables an efficient real-time seizure onset detection, which is integrated inside an implantable iEEG recording system for the treatment of epilepsy.

REFERENCES

[1] M. Stead *et al.*, "Microseizures and the spatiotemporal scales of human partial epilepsy," *Brain*, vol. 133, no. 9, pp. 2789–2797, Sep. 2010.
[2] J. Viventi *et al.*, "Flexible, foldable, actively multiplexed, high-density electrode array for mapping brain activity in vivo," *Nat. Neurosci.*, vol. 14, pp. 1599–1605, 2011.
[3] W. M. Chen *et al.*, "A fully integrated 8-channel closed-loop neural-prosthetic SoC for real-time epileptic seizure control," *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 286–287, Feb. 2013.
[4] S. S. Talathi *et al.*, "Non-parametric early seizure detection in an animal model of temporal lobe epilepsy," *J. Neural Eng.*, vol. 5, no. 1, pp. 85–98, Mar. 2008.
[5] A. M. Kamboh, M. Raetz, K. G. Oweiss, and A. J. Mason, "Area-power efficient VLSI implementation of multichannel DWT for data compression in implantable neuroprosthetics," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 2, pp. 128–135, Jun. 2007.
[6] A. Rodriguez-Perez, J. Ruiz-Amaya, M. Delgado-Restituto, and A. Rodriguez-Vazquez, "A low-power programmable neural spike detection channel with embedded calibration and data compression," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 2, pp. 87–100, Apr. 2012.
[7] F. Chen, A. P. Chandrakasan, and V. Stojanovic, "Design and analysis of a hardware-efficient compressed sensing architecture for data compression in wireless sensors," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 744–756, Mar. 2012.
[8] M. Shoaran, M. Hosseini Kamal, C. Pollo, P. Vandergheynst, and A. Schmid, "Compact low-power cortical recording architecture for compressive multichannel data acquisition," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 6, pp. 857–870, Dec. 2014.
[9] N. Verma *et al.*, "A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 804–816, Apr. 2010.
[10] J. Yoo *et al.*, "An 8-channel scalable EEG acquisition SoC with patient-specific seizure classification and recording processor," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 214–228, Jan. 2013.
[11] M. A. Davenport, P. T. Boufounos, M. B. Wakin, and R. G. Baraniuk, "Signal processing with compressive measurements," *IEEE J. Sel. Topics Signal Process.*, vol. 4, no. 2, pp. 445–460, Apr. 2010.
[12] L. Logesparan, A. J. Casson, and E. Rodriguez-Villegas, "Optimal features for online seizure detection," *Med. Biol. Eng. Comput.*, vol. 50, no. 7, pp. 659–669, Jul. 2012.
[13] K. Schindler, H. Leung, C. E. Elger, and K. Lehnertz, "Assessing seizure dynamics by analysing the correlation structure of multichannel intracranial EEG," *Brain*, vol. 130, pp. 65–77, Jan. 2007.
[14] K. A. Ng and Y. P. Xu, "A compact, low input capacitance neural recording amplifier," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 5, pp. 610–620, Oct. 2013.